

FEATURES

- 1 GHz to 18 GHz
- Compensation for Temperature Drift
- Input Regulators for Improved Stability
 - Versus Power Supply Variations
- 16 Bit Tuning Resolution
- -40 ℃ to +85 ℃ Temperature Range

YIG TUNED MULTIPLIERS WITH MILITARY SERIAL DRIVERS MS SERIES



DESCRIPTION

MICRO LAMBDA YIG Multipliers, model types MLHG Series are available with integrated serial driver circuits.

MICRO LAMBDA drivers eliminate the need for customers to design or develop their own driver circuits and sophisticated test and alignment procedures. Integrating a driver at MICRO LAMBDA's factory ensures that peak performance will be achieved at the time of manufacture. Alignment and compensation with the particular YIG filter can be maximized down to the component level.

All drivers in this series provide input voltage regulators, and compensation circuits to improve frequency drift.

Y SERIAL DRIVERS	1-18 GHz YTMs, MS SERIES
DRIVER INPUT & RESPONSE	SPECIFICATION (-40 to +85 deg. ℃)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	16 BIT Positive Logic (Fmax-Fmin)/65,535 Bit Resolution
Tuning Accuracy (excluding hysteresis)	See Table
Tuning Speed	5 mS for 1 GHz step to within ±10 MHz.
Main Driver Inputs	
Supply Voltage & Current	+15 V \pm .5 V @ Multiplier Tuning Current +50 mA, Max15 V \pm .5 V @ 50 mA
Supply Voltage Pushing	± 100 kHz, Max. @ ± .5 Vdc
Supply Voltage Ripple	10 mV Ripple Pk-Pk from 2 kHz to 3 MHz
Ground	Chassis Ground
YIG Heater Voltage & Current	+24 Vdc ±4 Vdc @ 300 mA surge for 2 seconds, 25 mA steady state Polarity independent: ±12 Vdc or ±15 Vdc acceptable
Digital Interface	The MLWI digital driver interface is a standard 3-wire connection compable with SPI/QSPI/MICROWIRE interfaces. The 3-wire serial interfwill operate in a 5V or 3.3V logic system. The chip-select in (CSELECTn) frames the serial data loading at the data input pin (DATI Immediately following CSELECTn's high-to-low transition, the data is sled synchronously and latched into the input register on the rising edge the serial-clock input (CLOCK). After 16 data bits have been loaded the serial input register, it transfers its contents to the DAC latch on CLECTn's low-to-high transition (Figure 2). Note that if CSELECTn d not remain low during the entire 16 CLOCK cycles, data will be corrupt in this case, reload the DAC latch with a new 16-bit word.

MS-SERIES — CONT.

YIG Tuned Multipliers with Military Serial Drivers

Power-On Reset

The MLWI digital driver has a power-on reset circuit to set the DAC's output to OV(F-min) in unipolar mode when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss.

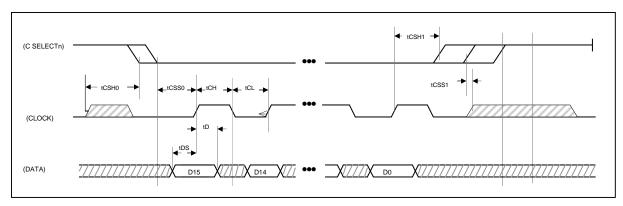


Figure 1. Timing Diagram

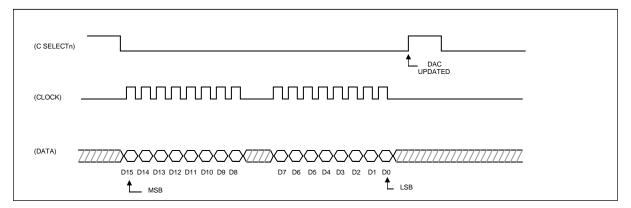


Figure 2. 3-Wire Interface Timing Diagram

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX	UNITS
CLOCK Frequency	fCLK		10	MHz
CLOCK Pulse Width High	tCH		45	ns
CLOCK Pulse Width Low	tCL		45	ns
CSn Low to CLOCK High Setup	tCSS0		45	ns
CSn High to CLOCK High Setup	tCSS1		45	ns
CLOCK High to CSn Low Hold	tCSH0		30	ns
CLOCK High to CSn High Hold	tCSH1		45	ns
DATA to CLOCK High Setup	tDS		40	ns
DATA to CLOCK High Hold	tDH		0	ns
VDD High to CSn Low (power-up delay)			20	μs

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YIG TUNED MULTIPLIERS WITH MILITARY SERIAL DRIVERS MS SERIES – CONTINUED

MODEL	Output Freq.	Input Freq.	Output Power	Accuracy	Current	Current	Outline
NUMBER	(GHz)	(MHz)	(dBm)	(MHz) *	+15V (mA)	-15V (mA)	Drawing
Multi-Octave Bands							
MLHG-1212MS	1.0-12.4	100	-30	±15	720	100	31-015
MLHG-2212MS	1.0-12.4	200	-25	±15	720	100	31-015
MLHG-5212MS	1.0-12.4	500	-13	±15	720	100	31-015
MLHG-1312MS	1.0-12.4	1000	-15	±15	720	100	31-015
Wideband							
MLHG-1218MS	1-18	100	-40	±20	1000	100	31-015
MLHG-2218MS	1-18	200	-35	±20	1000	100	31-015
MLHG-5218MS	1-18	500	-28	±20	1000	100	31-015
MLHG-1018MS	2-18	100	-37	±20	1000	100	31-015
MLHG-2018MS	2-18	200	-30	±20	1000	100	31-015

^{*} Accuracy includes frequency drift and linearity errors over the temperature range.

OUTLINE DRAWING: 31-015

